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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,939	08/27/2003	Robert A. Penchuk	A0312.70480 US00	5934

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Steven J. Henry
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, MA 02210

EXAMINER	
LE, VU ANH	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,939	PENCHUK, ROBERT A.	
	Examiner	Art Unit	
	Vu A. Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-13* is/are allowed.

6)☒ Claim(s) *1 and 4-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Itoh (5,220,530).

Itoh (Fig.2, col.1, lines 24-26) discloses a memory cell, comprising: a charge storage element (charge storage layer 35, col.1, line 38), a one-transistor switch (34, col.1, lines 28-32) constructed and arranged to selectively connect the storage element to a first data line (40), responsive to a first select signal (39), and a one-transistor gain element (33) having an input connected to receive a signal from the storage element and constructed and arranged to selectively provide a corresponding output signal to a second data line (read BL 37), the gain element comprising a FET (the gain transistor is MOSFET, col.1, line 32) having a first terminal (the gate terminal) connected to the storage element, a second terminal (the source/drain terminal) connected to the second data line and a third terminal (the drain/source terminal) selectively connected to one of a first power supply and a second power supply, the FET being symmetrical with respect to the second and third terminals (in MOSFET technology, the drain and

source terminals are interchangeable due to its symmetry), wherein the switch transfers a signal from the first data line onto the storage element and transfers a signal from the storage element onto the first data line when selected by the first select signal (see col.1).

3. Claims 1, 4-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Butler (5,513,139).

Butler (Fig.4A) discloses a memory cell, comprising: a charge storage element (charge storage layer 35), a one-transistor switch (T1) constructed and arranged to selectively connect the storage element to a first data line (30), responsive to a first select signal (28), and a one-transistor gain element (T2) having an input connected to receive a signal from the storage element and constructed and arranged to selectively provide a corresponding output signal to a second data line (31), the gain element comprising a FET (the picture showing CMOS FET transistor) having a first terminal (the gate terminal) connected to the storage element, a second terminal (the source/drain terminal) connected to the second data line and a third terminal (the drain/source terminal) selectively connected to one of a first power supply and a second power supply, the FET being symmetrical with respect to the second and third terminals (in MOSFET technology, the drain and source terminals are interchangeable due to its symmetry), wherein the switch transfers a signal from the first data line onto the

storage element and transfers a signal from the storage element onto the first data line when selected by the first select signal.

Butler (in Abstract) teaches a method of addressing an array of memory cells, comprising a write address decoder for writing groups of bits linearly arrayed with respect to each other (in first direction) and a read address decoder for reading groups of bits linearly arrayed with respect to each other and orthogonally disposed to the groups of bits written (in second direction, opposite the first direction).

Allowable Subject Matter

1. Claims 11-13 are allowed.

The independent claim 11 recites a gain memory cell consisting essentially of a charge storage element and two transistors which is different from the PRIOR ART teaching a charge storage element and three transistors.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Matsumura et al (4,935,896) discloses a gain memory cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu A. Le
Primary Examiner
Art Unit 2824

06/24/05